

What is claimed is:

1. A shift-register circuit having a plurality of
2 shift-register units connected in serial enabling
3 transmission of a clock signal, an inverse clock signal,
4 and a first voltage, each of the shift-register units
5 comprising:

6 a first transistor having a gate coupled to the
7 inverse clock signal and a first source/drain
8 coupled to a signal output from a previous-
9 stage shift-register unit;

10 an inverter having a first input terminal coupled to
11 the first source/drain of the first transistor;

12 a second transistor having a gate coupled to a
13 second source/drain of the first transistor and
14 a first source/drain coupled to the clock
15 signal and a second source/drain coupled to an
16 output terminal;

17 a third transistor having a gate coupled to a first
18 output terminal of the inverter and a first
19 source/drain coupled to the output terminal and
20 a second source/drain coupled to the first
21 voltage; and

22 a fourth transistor having a gate coupled to a
23 signal output from a next-stage shift-register
24 unit and a first source/drain coupled to the
25 output terminal and a second source/drain
26 coupled to the first voltage.

1 2. The shift-register circuit as claimed in claim
2, wherein the inverter comprises:

3 a fifth transistor having a gate and first
4 source/drain coupled to the inverse clock
5 signal and a second source/drain coupled to the
6 gate of the third transistor; and

7 a sixth transistor having a gate coupled to the
8 first source/drain of the first transistor and
9 a first source/drain coupled to the gate of the
10 third transistor and a second source/drain
11 coupled to the first voltage.

1 3. The shift-register circuit as claimed in claim
2, further comprising; a first capacitor connected
3 between the gate and second source/drain of the second
4 transistor.

1 4. The shift-register circuit as claimed in claim
2, wherein the transistors are MOS thin film transistors.

1 5. The shift-register circuit as claimed in claim
2, wherein the transistors are MOS thin film transistors.

1 6. A shift-register circuit having a plurality of
2 shift-register units connected in serial enabling
3 transmission of a clock signal, an inverse clock signal,
4 and a first voltage, each of the shift-register units
5 comprising:

6 a first transistor having a gate coupled to the
7 inverse clock signal and a first source/drain

8 coupled to a signal output from a previous-
9 stage shift-register unit;
10 a second transistor having a gate coupled to a
11 second source/drain of the first transistor and
12 a first source/drain coupled to the clock
13 signal and a second source/drain coupled to an
14 output terminal;
15 an inverter having a first input terminal coupled to
16 the output terminal;
17 a third transistor having a gate coupled to a first
18 output terminal of the inverter and a first
19 source/drain coupled to the output terminal and
20 a second source/drain coupled to the first
21 voltage; and
22 a fourth transistor having a gate coupled to a
23 signal output from a next-stage shift-register
24 unit and a first source/drain coupled to the
25 output terminal and a second source/drain
26 coupled to the first voltage.

1 7. The shift-register circuit as claimed in claim
2 6, wherein the inverter comprises:

3 a fifth transistor having a gate and first
4 source/drain coupled to a trigger signal and a
5 second source/drain coupled to the gate of the
6 third transistor; and
7 a sixth transistor having a gate coupled to the
8 output terminal and a first source/drain
9 coupled to the gate of the third transistor and

10 a second source/drain coupled to the first
11 voltage.

1 8. The shift-register circuit as claimed in Claim
2 7, wherein the trigger signal is the inverse clock
3 signal.

1 9. The shift-register circuit as claimed in Claim
2 7, wherein the trigger signal is a second voltage and the
3 level of the second voltage is more than the level of the
4 first voltage.

1 10. The shift-register circuit as claimed in claim
2 6, further comprising; a first capacitor connected
3 between the gate and second source/drain of the second
4 transistor.

1 11. The shift-register circuit as claimed in claim
2 6, wherein the transistors are MOS thin film transistors.

1 12. The shift-register circuit as claimed in claim
2 7, wherein the transistors are MOS thin film transistors.

1 13. A shift-register circuit having a plurality of
2 shift-register units connected in serial enabling
3 transmission of a clock signal, an inverse clock signal,
4 and a first voltage, each of the shift-register units
5 comprising:

6 a first transistor having a gate coupled to the
7 inverse clock signal and a first source/drain
8 coupled to a trigger terminal;

9 an inverter having a first input terminal coupled to
10 the first source/drain of the first transistor;

11 a second transistor having a gate coupled to a
12 second source/drain of the first transistor and
13 a first source/drain coupled to the clock
14 signal and a second source/drain coupled to an
15 output terminal for outputting signals;
16 a third transistor having a gate coupled to a first
17 output terminal of the inverter and a first
18 source/drain coupled to the output terminal and
19 a second source/drain coupled to the first
20 voltage;
21 a fourth transistor having a gate coupled to a reset
22 terminal and a first source/drain coupled to
23 the output terminal and a second source/drain
24 coupled to the first voltage; and
25 a control device for regulating the direction of the
26 output signals, comprising:
27 a seventh transistor having a gate coupled to a
28 left signal directing the output signal of
29 the shift-register circuit leftward and a
30 first source/drain coupled to a signal
31 output from a previous-stage shift-
32 register unit and a second source/drain
33 coupled to the reset terminal;
34 a eighth transistor having a gate coupled to
35 the left signal and a first source/drain
36 coupled to a signal output from a next-
37 stage shift-register unit and a second
38 source/drain coupled to the trigger
39 terminal;

40 a ninth transistor having a gate coupled to a
41 right signal for directing the output
42 signal rightward and a first source/drain
43 coupled to the output signal output from
44 the previous-stage shift-register unit and
45 a second source/drain coupled to the
46 trigger terminal; and
47 a tenth transistor having a gate coupled to the
48 right signal and a first source/drain
49 coupled to the output signal output from
50 the next-stage shift-register unit and a
51 second source/drain coupled to the reset
52 terminal.

1 14. The shift-register circuit as claimed in claim
2 13, wherein the inverter comprises:

3 a fifth transistor having a gate and first
4 source/drain coupled to the inverse clock
5 signal and a second source/drain coupled to the
6 gate of the third transistor; and
7 a sixth transistor having a gate coupled to the
8 first source/drain of the first transistor and
9 a first source/drain coupled to the gate of the
10 third transistor and a second source/drain
11 coupled to the first voltage.

1 15. The shift-register circuit as claimed in claim
2 14, wherein the transistors are MOS thin film
3 transistors.

1 16. A shift-register circuit having a plurality of
2 shift-register units connected in serial enabling
3 transmission of a clock signal, an inverse clock signal,
4 and a first voltage, each of the shift-register units
5 comprising:

6 a first transistor having a gate coupled to the
7 inverse clock signal and a first source/drain
8 coupled to a trigger terminal;

9 a second transistor having a gate coupled to a
10 second source/drain of the first transistor and
11 a first source/drain coupled to the clock
12 signal and a second source/drain coupled to an
13 output terminal for outputting signals;

14 an inverter having a first input terminal coupled to
15 the output terminal;

16 a third transistor having a gate coupled to a first
17 output terminal of the inverter and a first
18 source/drain coupled to the output terminal and
19 a second source/drain coupled to the first
20 voltage;

21 a fourth transistor having a gate coupled to a reset
22 terminal and a first source/drain coupled to
23 the output terminal and a second source/drain
24 coupled to the first voltage; and

25 a control device for controlling the direction of
26 the output signals, comprising:

27 a seventh transistor having a gate coupled to a
28 left signal directing the output signal of
29 the shift-register circuit leftward and a

30 first source/drain coupled to a signal
31 output from a previous-stage shift-
32 register unit and a second source/drain
33 coupled to the reset terminal;
34 a eighth transistor having a gate coupled to
35 the left signal and a first source/drain
36 coupled to a signal output from a next-
37 stage shift-register unit and a second
38 source/drain coupled to the trigger
39 terminal;
40 a ninth transistor having a gate coupled to a
41 right signal for directing the output
42 signal rightward and a first source/drain
43 coupled to the output signal output from
44 the previous-stage shift-register unit and
45 a second source/drain coupled to the
46 trigger terminal; and
47 a tenth transistor having a gate coupled to the
48 right signal and a first source/drain
49 coupled to the output signal output from
50 the next-stage shift-register unit and a
51 second source/drain coupled to the reset
52 terminal.

17. The shift-register circuit as claimed in claim 16, wherein the inverter comprises:

a fifth transistor having a gate and first source/drain coupled to a trigger signal and a second source/drain coupled to the gate of the third transistor; and

7 a sixth transistor having a gate coupled to the
8 output terminal and a first source/drain
9 coupled to the gate of the third transistor and
10 a second source/drain coupled to the first
11 voltage.

1 18. The shift-register circuit as claimed in claim
2 17, wherein the trigger signal is the inverse clock
3 signal.

1 19. The shift-register circuit as claimed in claim
2 18, wherein the trigger signal is a second voltage and
3 the level of the second voltage is more than the level of
4 the first voltage.

1 20. The shift-register circuit as claimed in claim
2 16, wherein the transistors are MOS thin film
3 transistors.

1 21. The shift-register circuit as claimed in claim
2 17, wherein the transistors are MOS thin film
3 transistors.